CROMEMCO TU-ART DIGITAL INTERFACE

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INTRODUCTION

The Cromemco TU-ART (Twin Universal Asynchronous Receiver and Transmitter) provides two channels of duplex serial data exchange; two channels of parallel data exchange; and ten interval timers. Status information is available through polling or by interrupt. In addition, each interval timer activates an interrupt and two interrupt request lines are brought out for the user. The TU-ART has its own crystal-controlled clock and interfaces to the S-100 bus asynchronously so that CPU clock frequency is not critical. The TU-ART incorporates two TMS 5501 Nmos I/O Controller chips.

DEFINITIONS

Throughout this manual the two TMS 5501 chips will be referred to as "Device A" and "Device B". Device A (IC 4) is the leftmost chip. Device B (IC 5) is the rightmost chip. Device A is nearer the heat sink and drives serial connector J4 and parallel connector J2. Device B is located to the right of Device A and drives serial connector J5 and parallel connector J3.

SWITCH SELECTABLE OPTIONS

1. Device A Address. The base address of the ports associated with Device A is set with positions 6-3 of the DIP switch which determine the msb, 2msb, 3msb, and 4msb of the I/O address. Setting a switch "on" conditions the TU-ART to respond to a "Ø" in that address bit. The msb, 2msb, and 3msb also control D7, D6, and D5 of the TU-ARTs Z80 mode 2 Interrupt Acknowledge Response vector. Address bits A3, A2, A1, and AØ are decoded to select which control or data port is being accessed (see Figure 2).

2. Device B Address. The base address of the ports associated with Device B is set with positions 10-7 of the DIP switch which determine the msb, 2msb, 3msb, and 4msb of the I/O address. Setting a switch "on" conditions the TU-ART to respond to a "Ø" in that address bit.

3. Interrupt Mode. When this switch (position 1) is on, the TU-ART operates in the 8080 interrupt mode: one of eight "Restart" instructions is gated to the data bus during an Interrupt Acknowledge cycle. Since the TU-ART can interrupt from one of 16 different sources, it is necessary to poll the devices if the TU-ART is in 8080 mode (see page 21).

When switch position 1 is off, the TU-ART responds in Z80 mode 2. In this mode, the TU-ART supplies a byte to the data bus during Interrupt Acknowledge that is used as

the lower eight bits of a memory address. The Z80 supplies the upper eight bits from the I register and automatically reads the corresponding memory location, as well as the next location, to find the starting location of an interrupt routine. Refer to pages 18-20 and/or the Z80 CPU Reference manual for details.

4. Normal/Reverse Address. When this switch (position 2) is on, it allows Device A and Device B to swap base addresses by means of an output to one of the parallel ports (Software Address-Reverse). This allows either Device A or Device B to be driven by a software driver whose port assignments are frozen in memory. Setting the switch "on" connects the msb of Device A's parallel output port to the Reverse Address control so that addresses may be flipped under software control. To flip addresses, output a byte with D7 high to Device A's parallel output port. To return to normal addressing, output a byte with D7 low to Device B's parallel output port. When switch position 2 is off, the Address Reverse switch is disconnected from the parallel port.

The Address Reverse signal is brought out to pin 1 of J2 and J3. When the Address Reverse switch is on, pin 1 will show the state of the TU-ART: Pin 1 = 0 means Reverse Mode,
Pin 1 = 1 means Normal Mode.

When the Address Reverse switch is off, pin 1 of J2 or J3 may be grounded externally to place the TU-ART in reverse Mode (Hardware Address-Reverse). Do not ground pin 1 of J2 or J3 while the Reverse Address switch is on as this will conflict with operation of Device A's parallel port.

FIGURE 1

DIP SWITCH SETTINGS

Switch	Off	On
1	IM2 (Z8Ø Interrupts)	IMØ (8Ø8Ø Interrupts)
2	Hardware Address-Reverse	Software Address-Reverse
3	Bit 4 = 1, Device A	Bit 4 = Ø, Device A
4	Bit 5 = 1, Device A	Bit 5 = Ø, Device A
5	Bit 6 = 1, Device A	Bit 6 = Ø, Device A
6	Bit 7 = 1, Device A	Bit 7 = Ø, Device A
7	Bit 4 = 1, Device B	Bit 4 = Ø, Device B
8	Bit 5 = 1, Device B	Bit 5 = Ø, Device B
9	Bit 6 = 1, Device B	Bit 6 = Ø, Device B
10	Bit 7 = 1, Device B	Bit 7 = Ø, Device B

The standard settings of these switches are switch positions 1, 7, and 9 off, all others on. This selects Ø as the I/O base address of Device A, 5Ø hex as the I/O base address of Device B and enables Software Address-Reverse and the Z80 interrupt mode.

FIGURE 2

SUMMARY OF DATA AND CONTROL PORT ADDRESS FOR TU-ART[tm]

OFFSET	A7 A6 A5 A4 A3 A2 A1 AØ	FUNCTION
Ø	--Set by DIP switch at ----"A Base Address"-- Ø Ø Ø Ø	IN Device A status register
Ø		OUT Device A baud rate register
1		IN Device A receiver data register
1		OUT Device A transmitter data register
2		OUT Device A command register
3		IN Device A interrupt address register
3		OUT Device A interrupt mask register
4		IN Device A parallel port
4		OUT Device A parallel port
5		OUT Device A timer 1
6		OUT Device A timer 2
7		OUT Device A timer 3
8		OUT Device A timer 4
9		OUT Device A timer 5
Ø	--Set by DIP switch at ----"B Base Address"-- Ø Ø Ø Ø	IN Device B status register
Ø		OUT Device B baud rate register
1		IN Device B receiver data register
1		OUT Device B transmitter data register
2		OUT Device B command register
3		IN Device B interrupt address register
3		OUT Device B interrupt mask register
4		IN Device B parallel port
4		OUT Device B parallel port
5		OUT Device B timer 1
6		OUT Device B timer 2
7		OUT Device B timer 3
8		OUT Device B timer 4
9		OUT Device B timer 5

NOTES

All unassigned ports are free for system use (IN #2, OUTs #5-9. INs and OUTs #10-15).

If Device A and Device B are set to the same base address, Device A will override.

Device A (IC 4) is located leftmost.

Device B is IC 5

INTERRUPT PRIORITY CHAIN

When more than one TU-ART is used in a system, it is necessary to coordinate the Interrupt Responses in order to prevent bus conflict during Interrupt Acknowledge cycles. This is done by first connecting J1 PRIORITY OUT/ from the highest priority TU-ART to J1 PRIORITY IN/ of the next highest priority TU-ART , then connecting J1 PRIORITY OUT/ of the second TU-ART to J1 PRIORITY IN/ of the next TU-ART, and so on until all TU-ARTs are connected. The J1 PRIORITY IN/ pin of the highest priority board is left unconnected. Device A is internally prioritized over Device B on each TU-ART.

STATUS BIT SELECTION

The connection of status flag bits to data bits is done on the PC board at the location of the status socket below J3. Cromemco software conventions assign D6=Receiver Data Available (RDA), and D7=Transmitter Buffer Empty (TBE). For specialized assignments (like more than one bit per flag) see page 7.

Status Socket

The status flag bits available on input port Ø are connected to the data bits by foil traces in the "status socket" located between IC's 8 and 9.

The flag assignment used by all Cromemco software is discussed on page 9 under "Register Description".

If necessary, the flags may be assigned to different data bits. This may be most easily done as follows:

1. Notice that the flags are arranged along the left row of pads and that the data bits are arranged along the right side row of pads. Note also that only those 8 traces connecting the right and left pads are not covered by the solder mask. There are 5 traces which pass through this area which are covered.
2. Use a razor blade or similarly sharp knife to cut all 8 of the traces connecting the left and right rows of pads. Be very careful not to cut the traces which are covered by the solder mask.
3. Install and solder a 16 pin IC socket in the 2 rows of pads.
4. Install a 16 pin "component header" in the socket.
5. Using small (24 or 28 Awg) insulated wire connect the flags (on the left) to the desired data bits (on the right) on the component header.
6. The component header is now a "plug" for your particular flag assignment. Several different flag assignment "plugs" can be prepared in the same manner and used at different times to suit the requirements of the software being executed.

Any given flag may be assigned to more than one data bit. However, each data bit can have only one flag assigned to it.

INTERFACE OPTIONS

1. TTY 20 mA. To drive a Teletype, the following connections should be made (at J4 or J5 for Device A or B respectively):

Pin 23 Current into printer (ASR-33 pin 7)

Pin 25 Return current from printer (ASR-33 pin 6)

Pin 17 Current into keyboard (ASR-33 pin 4)

Pin 24 Return current from keyboard (ASR-33 pin 3).

2. RS/232C. An RS232 terminal (such as CRT) may be plugged into an interface cable directly out of J4 or J5. The TU-ART assumes the role of data-set (computer) in this case. See the cable diagram on page 31 for this connection.

3. Parallel I/O. The parallel port output drivers may be tristated by grounding pin 8 of the parallel port (J2,J3). A bidirectional bus may be implemented by simply wiring the input and output lines together and using pin 8 to control the direction of data flow. Pin 8 low implies data input to the TU-ART and pin 8 high implies data output from the TU-ART.

REGISTER DESCRIPTION

In the following sections, each I/O port (register) will be discussed. The operation of these ports is the same in Device A and Device B. Refer to page 25 for a summary.

OFFSET	IN/OUT	DESCRIPTION
Ø	IN	Status Register: Bit assignment by PC Board traces.

D7	D6	D5	D4	D3	D2	D1	DØ
Transmit Buffer Empty	Read Data Avail.	Int. Pend-ing	Start Bit Detect	Full Bit Detect	Ser-ial Rcv	Over-Run Err	Frame Error

The functions of these flags are indicated in the following sections.

D7 Transmitter Buffer Empty (TBE):

A high in bit 7 indicates that the transmitter data buffer is ready to accept a new byte. TBE goes high as soon as the serial transmitter begins to send the byte currently in the buffer. Since the transmitter is "double-buffered", the user may respond to the TBE signal and load the buffer even before the previous byte has been totally transmitted. TBE also activates interrupt request 5. TBE is cleared when the buffer is loaded and is set by the RESET command.

D6 Receiver Data Available (RDA):

A high in bit 6 indicates that a byte of data is available from the receiver buffer. This flag remains high until the

buffer is read. A RESET command clears the flag. If the buffer is not read by the time the next byte from the receiver is ready, the new byte will write over the old byte and the overrun error flag will be set. RDA also activates interrupt request 4.

D5 Interrupt Pending (IPG):

A high in bit 5 indicates that one or more of the eight interrupt request sources has become active. This flag goes high at the same time as the interrupt request pin of the TMS 5501.

D4 Start Bit Detect (SBD):

A high in bit 4 indicates that the serial receiver has detected a start bit. This bit remains high until the full character has been received. SBD is cleared by RESET command. This bit is provided for test purposes.

D3 Full Bit Detect (FBD):

The FBD flag in bit 3 goes high one full bit time after the start bit has been detected. This bit remains high until the full character has been received. FBD is cleared by a RESET command. This bit is provided for test purposes.

D2 Serial Receive (SRV):

A high in bit 2 indicates high level on the serial data input line. A low in bit 2 indicates a low level on the serial data input line. SRV is high when no data is being received. This bit is provided for break detection and for test purposes.

D1 Overrun Error (ORE):

A high in bit 1 indicates that the receiver has loaded the receiver data buffer before the previous contents were read. ORE is cleared after the status port is read or by the RESET command.

DØ Frame Error (FME):

A high in bit Ø indicates an error in one or both of the stop bits which "framed" the last received data byte. FME remains high until a valid character is received.

Ø OUT Baud rate register. Loading this register sets the baud rate and stop bits for serial receive and transmit data. Bit assignment is as follows:

D7	D6	D5	D4	D3	D2	D1	DØ
STOP BITS	96ØØ	48ØØ	24ØØ	12ØØ	3ØØ	15Ø	11Ø

D7 STOP

A high in bit 7 selects one stop bit for serial receive and transmit data. A low in bit 7 selects two stop bits.

D6-DØ BAUD RATE

A high in one of the lower seven bits selects the corresponding baud rate. If more than one bit is high, the highest rate selected will result. If none of the bits are high, the serial transmitter and receiver will be disabled. (For special purposes these baud rates can be octupled -- see the description of HBD in the command register).

1 IN Receiver Data. This register contains an assembled byte of data from the serial receiver

1 OUT Transmitter Data. This register is loaded with data for the serial transmitter.

2 IN Not Assigned. Reading this port causes no response from the TU-ART. This address is available for other parts of the computer system.

2 OUT Command Register. The format for the command register is as follows:

- - - - latched - - - -

D7	D6	D5	D4	D3	D2	D1	DØ
Not Used	Not Used	Test	HIGH BAUD	INTA Enable	RST7 Sel.	Break	Reset

D5 Test Bit (TB5):

A high in bit 5 disables the internal interrupt priority logic and then enables the internal clock. Thus, the signal on the INT pin of the 5501 becomes a TTL level clock of 1562.5 Hz (12.5 kHz if HBD is high -- see D4 High Baud below). TB5 should be low for normal operation.

D4 High Baud (HBD)

A high in bit 4 octuples the rate of the internal clock. This causes the interval timers to count eight times faster and the serial data rates to increase eight-fold. When bit 4 is high, baud rates up to 76.8k are available for high speed data transfers.

D3 INTA Enable (INE):

A high in bit 3 allows the 5501 to respond to an

Interrupt Acknowledge by gating a Restart instruction into the data bus at the correct time and resetting its internal interrupt request latch.

A low in bit 3 prevents the 5501 from detecting an INTA cycle. Bit 3 should be high for normal operation.

D2 RST7 Select (RS7):

A high in bit 2 connects the MSB of the parallel input port to the interrupt request latch for the lowest priority interrupt (interrupt 7). A low-to-high transition on the MSB of the parallel input port (PI7) will activate the interrupt request latch.

A low in bit 2 connects the output of Timer 5 to the interrupt request latch for the lowest priority interrupt (interrupt 7). When the timer count reaches zero, the interrupt request latch will be activated.

D1 Break (BRK):

A high in bit 1 holds the serial transmitter output in the low state (spacing). RES will override (see DØ Reset below).

A low in bit 1 allows normal operation. BRK should be low for normal operation.

DØ Reset (RES):

A high in bit Ø causes the following actions:

a) The Serial Receiver goes into search mode; RDA, SBD, FBD, and ORE are set to zero. The contents of the receiver buffer are not affected.

b) The Serial transmitter output is set high (marking). If DØ and D1 are both high, the RES function will override. RES sets TBE high.

c) The interrupt register is cleared except for the TBE interrupt request which is set high.

d) The interval timers are cleared.

. RES is not latched.

ØЗ IN Interrupt Address: This register contains the encoded address of the highest priority interrupt currently requesting service. This address is identical to the "Restart" instruction op-code for the interrupt acknowledge. Thus, the register contents may be (in order of service priority):

HEX		SOURCE
C7	- - - -	Timer 1
CF	- - - -	Timer 2
D7	- - - -	Sens/
DF	- - - -	Timer 3
E7	- - - -	Receiver Data Available
EF	- - - -	Transmitter Buffer Supply
F7	- - - -	Timer 4
FF	- - - -	Timer 5 or PI7

This register is provided for servicing interrupts via polling. After the register is read, the corresponding bit in the interrupt request register is reset. If the register is read when no interrupt is pending, it will read ØFFH.

Ø3 OUT Interrupt Mask: The contents of this register are logically "And"-ed with output from the interrupt request register on the 5501. A high bit in the interrupt mask allows the corresponding request to pass on into the priority encoder. A low bit in the interrupt mask inhibits the corresponding interrupt from passing any further. Since the interrupt requests are latched independently of the state of the mask, an interrupt may be requested while the mask bit is low. The request will be retained until the mask is changed and the request allowed to pass on (assuming no RES command in the interim). The mask bit assignments are:

D7	D6	D5	D4	D3	D2	D1	DØ
Timer5	Timer4	TBE	RDA	Timer3	Sens/ P17	Timer2	Timer1

Ø4 IN Parallel Input: This register contains the data presented at J2 (Device A) or at J3 (Device B). The input data must be stable 75 ns after Input Strobe/ goes low. The peripheral supplying data to the TU-ART can indicate data available by activating the SENS/ line (or by raising the MSB of the parallel input if the RS7 bit in the command register is high).

When using Z80 block input commands, it is not necessary to supply data at full speed. The input peripheral should simply pull down the WAIT/ line (pin 21 of J1 or J3) whenever Input Strobe/ goes low

and should not let WAIT/ go high until the next byte is presented to the TU-ART. (The TU-ART will not read this byte until Input Strobe/ goes low again).

Ø4 OUT Parallel Output: This register contains the data which drives the parallel output buffers. The output data is guaranteed stable 1.45 μsec after the falling edge of Output Strobe/. The TTL output buffers which drive J2 (Device A) and J3 (Device B) may be put in a high-impedance state by pulling down on Disable/ (pin 8).

When using the Z80 block output commands, it is not necessary to receive data at full speed. The output peripheral should simply pull down the WAIT/ line (pin 21 of J2 or J3) whenever Output Strobe/ goes low and not let WAIT/ go high until the output peripheral has had time to "digest" the data.

Ø5 IN Not Connected: Addressing this port causes no response from the TU-ART. This address is available for use by other parts of the computer system.

Ø5 OUT Timer 1: This register contains the count used to start Timer 1. This count is decremented by 1 every 64 μseconds after initial loading. When the count reaches zero, bit Ø of the interrupt request register is set and the timer disabled. Since the maximum count is 255, the longest interval is 255x64 μsec. = 16.32 msec. Accuracy is plus Ø and minus 64 μsec.

Loading a count of zero causes an immediate interrupt request to the interrupt request register. Loading a new count while the timer is counting reinitializes the timer without an interrupt request. If HBD is high in the command register, the timers will count 8 times as fast.

Ø6	IN	Not Connected: Same as Input Ø5.
Ø6	OUT	Timer 2: Operates in the same fashion as timer 1.
Ø7	IN	Not Connected: Same as Input Ø5.
Ø7	OUT	Timer 3: Operates in the same fashion as timer 1.
Ø8	IN	Not Connected: Same as Input Ø5.
Ø8	OUT	Timer 4: Operates in the same fashion as timer 1.
Ø9	IN	Not Connected: Same as Input Ø5.
Ø9	OUT	Timer 5: Operates in the same fashion as timer 1.

OAH - ØFFH IN and OUT Not Connected: Same as Input Ø5.

Remember that the INE bit in the status register must be high for correct operation of Interrupt Acknowledge cycles. Also, be sure that the Z80 has executed the interrupt mode setting command ØED5EH ("IM2") and the interrupt enable command ØFBH ("EI"). A Reset input to the Z80 will necessitate both of these operations.

Assuming that both the Z80 and the TU-ART have been initialized, the sequence following reception of a byte of serial data at Device B would be as follows:

a) The assembled byte is loaded into the receiver data buffer.

b) The RDA status bit is set and the interrupt request register (bit 3) is set.

c) If bit 3 of the interrupt mask of the Device in question is a one, the request passes on to the priority encoder. If bit 3 is a zero, no further action occurs until the mask is changed.

d) The priority encoder compares all incoming interrupt requests and sets its output to the value of the highest priority incoming interrupt. Thus, since Device B receives the serial data byte in our example; the priority encoder will set its output to "priority 3" if Timers 1, 2, 3, and SENSB/ from Device B are inactive or masked out.

e) Device B's INT pin goes high, which in turn pulls down $\overline{\text{PINT}}$ on the S-100 bus.

f) The Z80 checks the interrupt line at the end of the current instruction, and finding the line active, goes into an Interrupt Acknowledge (INTA) cycle.

g) The occurence of the INTA cycle is detected by the TU-ART which then transmits PRIORITY OUT/ = 0 to connector J1. This temporarily disables Interrupt Acknowledge from lower priority boards. If no board with higher priority is holding down PRIORITY IN/, and if Device A has no interrupt pending, then Device B gates onto the data bus the proper Z80 INTA response vector. In this example, Device B would place on the data bus 18H (logically "OR"ed with A7, A6, A5 Ø Ø Ø Ø Ø from Device A's Base Address). The corresponding bit in the interrupt request latch is reset.

h) The Z80 reads the INTA response byte and appends it to the byte in the I register. This then forms a sixteen bit address which points to the first of two sequential bytes in memory which in turn designate the actual starting address of the service routine. The CPU automatically executes a CALL to the starting address.

OPERATION USING 8080 MODE INTERRUPTS

When the TU-ART is used with 8080 processors, it is necessary to "chain" Device B through the SENS input on Device A. This requires one of the eight 8080 INTA responses, RST2 (ØD7H), to be serviced by a routine which polls the status and interrupt address registers of Device B. The remaining seven 8080 INTA responses are serviced immediately. The resulting priority assignment is as follows:

Priority	TU-ART's (hex) 8080 INTA Response	Source of Interrupt
15	C7 (RSTØ)	Device A, Timer 1
14	CF (RST1)	Device A, Timer 2
13	D7 (RST2)	Device B, Timer 1
12	"	" Timer 2
11	"	" SENSB/
10	"	" Timer 3
9	"	RDA
8	"	" TBE
7	"	" Timer 4
6	"	" Timer 5/ P17
5	"	" SENSA/
4	DF (RST3)	Device A, Timer 3
3	E7 (RST4)	" RDA
2	EF (RST5)	" TBE
1	F7 (RST6)	" Timer 4
Ø	FF (RST7)	" Timer 5/ P17

It is, of course, possible to use the interrupt mask of each Device to selectively enable and disable the sources of interrupts (see the description of output port 3).

It is not necessary to reset the INE status bit of Device B to zero even though Device B can never respond directly to an Interrupt Acknowledge (INTA) cycle. The INTA status information is not fed to Device B if 8080 mode INTA has been selected on

the Option DIP Switch. Therefore, the 5501 never attempts to drive the bus during INTA.

No wiring changes are necessary to disconnect the INT pin of Device B from the $\overline{\text{PINT}}$ driver and to connect it to the Device A SENS pin. All this is done automatically when 8080 mode INTA has been selected on the Option DIP Switch. Note that SENSA/ at J1 is still connected. Pulling this line down will generate an interrupt request. The 8080 must execute the EI instruction (ØFBH) after resets or interrupts before an interrupt may take place.

For the 8080, the sequence of events corresponding to Device B receiving a byte of serial data are as follows:

a) The assembled byte is loaded into the receiver data buffer.

b) The RDA status bit is set, the interrupt request register bit 3 is set, and the IPG status bit is set in the device which received the character (Device B in this example).

c) If bit 3 of the interrupt mask of the device in question is a one, the interrupt request passes on to the priority encoder. If bit 3 is a zero, no further action occurs until the mask is changed.

d) The priority encoder compares all incoming interrupt requests and sets its output to the value of the highest priority incoming interrupt. Thus, if Device B received the serial data byte in our example, the priority encoder will set its output to priority three

if and only if Device B's Timers 1, 2, and 3 and SENSB/ are inactive or masked out.

e) Device B's INT pin goes high which in turn activates the SENS pin of Device A.

f) If bit 2 of Device A's interrupt mask is a one, the interrupt request will pass on to the priority encoder. If bit 2 is a zero, no further action occurs until the mask is changed.

g) The priority encoder in Device A compares all incoming interrupt requests and sets its output to the value of the highest priority incoming interrupt. In our example, the interrupt from Device B activates the SENS input at Device A. This interrupt will have top priority if and only if Device A's Timers 1 and 2 are inactive or masked out..

h) Device A's INT pin goes high which in turn pulls down $\overline{\text{PINT}}$ on the S-100 bus.

i) The 8080 checks the interrupt line at the end of the current instruction and, finding it active, goes into an Interrupt Acknowledge (INTA) cycle.

j) The occurence of the INTA cycle is detected by the TU-ART which then transmits PRIORITY OUT/ = 0 to J1. This temporarily disables Interrupt Acknowledge from lower priority boards. If no board with high priority is holding down PRIORITY IN/, Device A will gate an 8080 INTA response onto the bus. In this example, Device A would place on the data bus D7H(RST2).

The corresponding bit in Device A's interrupt request register is reset.

k) The 8080 reads the INTA response byte and performs a CALL to location 1ØH.

1) The service routine located at starting location 1ØH, reads the status register of Device B. If IPG is zero, no interrupts are pending in Device B so that the interrupt request must have originated from the SENSA/ line. The service routine branches to the appropriate subroutine.

If IPG is one, Device B has an interrupt pending which must be serviced. The source of the interrupt is determined by reading Device B's Interrupt Address register. In our example, the Interrupt Address register would contain E7H. When this byte is read, the corresponding bit of the interrupt request register will be reset. The service routine has now determined the true cause of the interrupt and branches to the appropriate subroutine.

FIGURE 2

SUMMARY OF REGISTER FORMATS FOR TU-ART, EACH DEVICE

OFFSET	FUNCTION	D7	D6	D5	D4	D3	D2	D1	DØ	REF. PAGE
Ø	IN STATUS	TBE	RDA	IPG	SBD	FBD	SRV	ORE	FME	9-11
Ø	OUT STATUS	STOP	96ØØ	48ØØ	24ØØ	12ØØ	3ØØ	15Ø	11Ø	11
1	IN SERIAL	MSB	Direction of shift---→						LSB	12
1	OUT SERIAL	MSB	Direction of shift---→						LSB	12
2	OUT COMMAND	--	--	TB5	HBD	INE	RS7	BRK	RES	12-14
3	IN INT ADDR	1	1	I4*	I2*	IØ*	1	1	1	14
3	OUT INT MASK	T5/P17	T4	TBE	RDA	T3	SENS	T2	T1	15
4	IN PARALLEL	MSB							LSB	15-16
4	OUT PARALLEL	MSB							LSB	16
5-9	OUT Timer1-5	MSB	(Delay=count x 64 μsec, HBD=0)						LSB	16-17
			(Delay=count x 8 μsec, HDB=1)							

* I4	I2	IØ	Source of Interrupt
Ø	Ø	Ø	Timer 1
Ø	Ø	1	Timer 2
Ø	1	Ø	SENS
Ø	1	1	Timer 3
1	Ø	Ø	RDA
1	Ø	1	TBE
1	1	Ø	Timer 4
1	1	Ø	Timer 5/ P17

CONNECTING THE TU-ART TO I/O DEVICES

J2 PARALLEL A

Pin	Name	Signal Direction	Voltage Level	Function
1	$\overline{\text{Invert}}$	Input	TTL	Used for normal/reverse address switching. See discussion on page 3.
2	$\overline{\text{Input Strobe A}}$	Output	TTL	When active indicates that the data present on input bits Ø-7 is being sampled.
3	Vcc	Output	+5V	
4	Bit 6	Input	TTL	
5	4	Input	TTL	
6	2	Input	TTL	
7	Ø	Input	TTL	
8	$\overline{\text{Disable}}$	Input	TTL	Turns the output drivers for the parallel output bits off.
9	$\overline{\text{Output Strobe}}$	Output	TTL	Indicates that data is present on parallel output bits Ø-7.
10	Bit 6	Output	TTL	
11	4	Output	TTL	
12	2	Output	TTL	
13	Ø	Output	TTL	
14	Signal Ground	Output	ØV	
15	$\overline{\text{SENS A}}$	Input	TTL	Interrupt request, input to IC 4 5501 (A)
16	Bit 7	Input	TTL	
17	5	Input	TTL	
18	3	Input	TTL	
19	1	Input	TTL	
20	$\overline{\text{NMI}}$	Input	TTL	Non maskable interrupt. This pin is tied directly to pin 12 of the S-100 bus. Consult the Z-80 manual for use. Only usable with the Cromemco ZPU card.
21	$\overline{\text{Wait}}$	Input	TTL	This pin is tied directly to Pin 72 (PRDY) of the S-100 bus. Stops the CPU when active.

Pin	Name	Signal Direction	Voltage Level	Function
22	Bit 7	Output	TTL	
23	5	Output	TTL	
24	3	Output	TTL	
15	1	Output	TTL	

J3 PARALLEL B

Pin	Name	Signal Direction	Voltage Level	Function
1	$\overline{\text{Invert}}$	Input	TTL	Used for normal/reverse address switching. See discussion on page
2	$\overline{\text{Input Strobe B}}$	Output	TTL	When active indicates that the data present on input bits Ø-7 is being sampled.
3	Vcc	Output	+5V	
4	Bit 6	Input	TTL	
5	4	Input	TTL	
6	2	Input	TTL	
7	Ø	Input	TTL	
8	$\overline{\text{Disable}}$	Input	TTL	Turns the output drivers for the parallel output bits off.
9	$\overline{\text{Output Strobe}}$	Output	TTL	Indicates that data is present on parallel output bits Ø-7.
10	Bit 6	Output	TTL	
11	4	Output	TTL	
12	2	Output	TTL	
13	Ø	Output	TTL	
14	Signal Ground	Output	ØV	
15	$\overline{\text{SENS B}}$	Input	TTL	Interrupt request, input to IC 5 5501 (B).
16	Bit 7	Input	TTL	
17	5	Input	TTL	
18	3	Input	TTL	
19	1	Input	TTL	
20	$\overline{\text{NMI}}$	Input	TTL	Non maskable interrupt. This pin is tied directly to pin 12 of the S-100 bus. Consult the Z-80 manual for use. Only usable with the Cromemco ZPU card.
21	$\overline{\text{Wait}}$	Input	TTL	This pin is tied directly to pin 72 ($\overline{\text{PRDY}}$) of the S-100 bus. Stops the CPU when active.
22	Bit 7	Output	TTL	
23	5	Output	TTL	
24	3	Output	TTL	
25	1	Output	TTL	

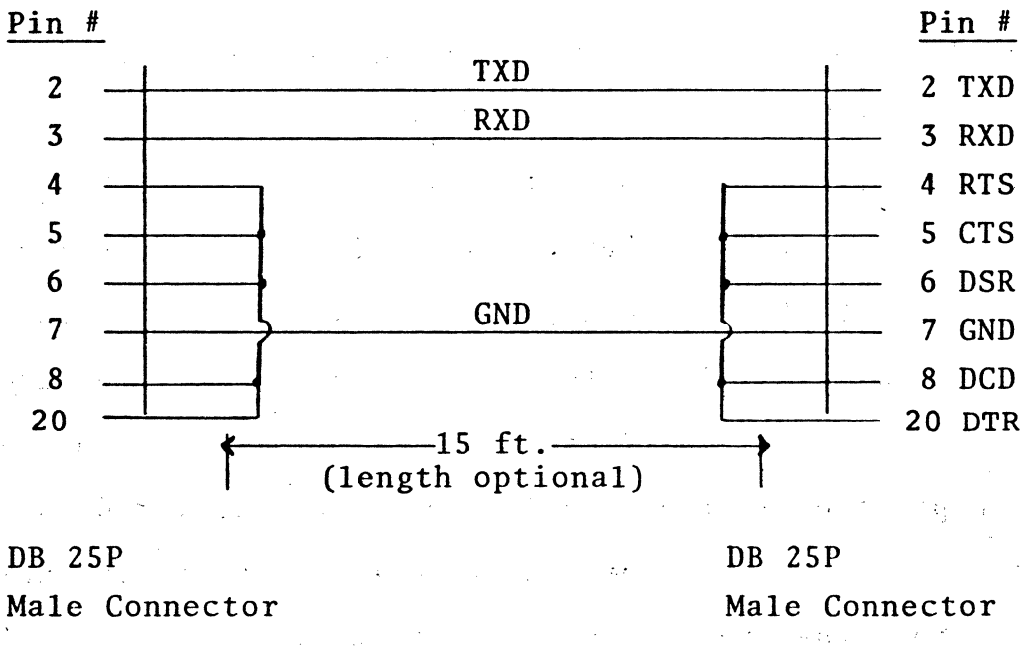
J4 SERIAL A

Pin	Name	Signal Direction	Voltage Level	Function
1	FRAME GROUND	-	-	Not connected on PC board This pin should be tied to the chassis at the back panel if an RS232 terminal is being used.
2	INPUT A	Input	±12V	RS232 data input.
3	OUT A	Output	±12V	RS232 data output.
4	NC			
5	NC			
6	DSR	Output	+12V	RS232 data set ready. Tied to +12V through 1.5k (R5) on PC board.
7	SIGNAL GND	-	0V	RS232 signal ground
8	CTS	Output	+12V	RS232 clear to send. Tied to +12V through 1.5k (R4) on PC Board.
9-16	NC			
25	TTY OUT A	Output	-	Data output current loop - (current sink)
23	TTY OUT A	Output	+12V	Data output current loop + (current source)
17	TTY IN A	Input	+12V	Data input current loop + (current source)
24	TTY IN A	Input	-5V	Data input current loop - (current sink)
18-22	NC			
25-26	NC			

J5 SERIAL B

Pin	Name	Signal Direction	Voltage Level	Function
1	FRAME GROUND	-	-	Not connected on PC board. This pin should be tied to the chassis at the back panel if an RS232 terminal is being used.
2	INPUT B	Input	±12V	RS232 data input
3	OUT B	Output	±12V	RS232 data output
4	NC			
5	NC			
6	DSR	Output	+12V	RS232 data set ready. Tied to +12V through 1.5k (R5) on PC board.
7	SIGNAL GND	-	0V	RS232 signal ground
8	CTS	Output	+12V	RS232 clear to send. Tied to +12V through 1.5K (R4) on PC board.
9-16	NC			
25	TTY OUT B	Output	-	Data output current loop - (current sink)
23	TTY OUT B	Output	+12V	Data output current loop + (current source)
17	TTY IN B	Input	+12V	Data input current loop + (current source)
24	TTY IN B	Input	-5V	Data input current loop - (current sink)
18-22	NC			
25-26	NC			

TERMINAL TO TU-ART CABLE



This is a diagram of the cable required to connect a serial RS-232 I/O device (such as a CRT terminal) from the DB 25-S socket of the TU-ART cable (model TRT-CBL) to the DB 25-S connector of the RS-232 device.

ORIGINATE MODE MODIFICATION

The TU-ART is factory wired for answer mode on both A and B serial I/O channels. This means that RS232 serial data is input to the TU-ART on J4 pin 3 (Channel A) or J5 pin 3 (Channel B), and that serial data is output from the TU-ART on J4 pin 2 (Channel A) or J5 pin 2 (Channel B).

The TU-ART can be configured for originate mode (that is, assume the role of terminal) by reversing the direction of data flow on pins 2 and 3 of J4 and/or J5. Pads have been provided in the area between J4 and J5 for doing this. The modification can be made to either or both channels.

Note that there are two vertical rows of pads. Those closest to J4 are labeled A and affect Channel A only while those closest to J5 are labeled B and affect Channel B only.

The uppermost pad is connected to pin 2 of the DB-25 connector and is also connected by a short foil trace on the solder side of the board to the bottom pad. The bottom pad is connected to a data output driver (IC 9). The pad second from the top is connected to pin 3 of the DB-25 connector and is also connected by a short foil trace on the soler side to the pad 3rd form the top. The pad third from the top (labeled "in") is connected to a data receiver (IC 11).

To modify the board for originate mode, proceed as follows: (The modification is the same for both channels)

1. Cut the trace connecting the top and bottom pads on the solder side. (For Channel A be certain to cut the trace between 2 pads and not the trace between

the bottom pad and IC 9 Pin 4).

2. Cut the trace between the pad 2nd from the top and the pad 3rd from the top.
3. Connect a jumper from the bottom pad (out) to the pad 2nd from the top.
4. Connect a jumper from the pad 3rd from the top (in) to the top pad.

SPARE RS232 DRIVERS AND RECEIVERS.

There are two uncommitted sections in IC 9, A 75189 driver. Pads for jumper wires have been provided at pins 1, 2, 3 and at pins 11, 12, 13.

There are two uncommitted sections on IC 11, A 75188 Receiver. Pads have been provided at pins 4, 5, 6 and at pins 8, 9, 10.

These uncommitted sections are shown on the schematic diagram.

```
                        0002 ;
                        0003 ; RINGS THE CONSOLE BELL AT 1-SECOND INTERVALS.
                        0004 ; SET SWITCHES 1, 7, AND 9 OFF, ALL OTHER
                        0005 ; SWITCHES ON THE TUART DIP SWITCH ON.
                        0006 ; SET CONSOLE TERMINAL BAUD RATE TO 9600.
                        0007 ; CONNECT TERMINAL TO TUART CONNECTOR J4,
                        0008 ; (SERIAL A).
                        0009 ;
0000                    0010        ORG     100H
                        0011 ;
0100 F3                 0012        DI
0101 310003             0013        LD      SP,300H
0104 3E00               0014        LD      A,0         ;SELECT DEVICE A  (SEE
0106 D354               0015        OUT     54H,A       ;SOFTWARE ADDR-REVERSE).
0108 3E09               0016        LD      A,9         ;RESET DEVICE A & ENABLE
010A D302               0017        OUT     2,A         ;INTERRUPT ACK. RESPONSE.
010C 3EC0               0018        LD      A,0C0H      ;SET BAUD RATE
010E D300               0019        OUT     0,A         ;TO 9600.
0110 3E01               0020        LD      A,1         ;MASK OUT ALL INTERRUPTS
0112 D303               0021        OUT     3,A         ;BUT THOSE FROM TIMER1,
                        0022 ;                          ;DEVICE A.
0114 3E00               0023        LD      A,0         ;MASK OUT ALL INTERRUPTS
0116 D353               0024        OUT     53H,A       ;FROM DEVICE B.
0118 3E02               0025        LD      A,2         ;SELECT PAGE 2
011A ED47               0026        LD      I,A         ;FOR INTERRUPT VECTORS.
011C ED5E               0027        IM2                 ;INTERRUPT MODE 2.
                        0028 ;
011E CD2C01             0029        CALL    INIT        ;INITIALIZE THE TIMER.
                        0030 ;
                        0031 ; WHAT FOLLOWS IS AN INFINITE LOOP.  IT COULD
                        0032 ; INSTEAD BE SOME USEFUL PROGRAM ENTIRELY UN-
                        0033 ; RELATED TO THE TIMER PROGRAM.
                        0034 ;
0121 C32101             0035 HERE:  JP      HERE
                        0036 ;
                        0037 ;
                        0038 ; INTERRUPT SERVICE ROUTINE.
                        0039 ;
0124 05                 0040 TIMER: DEC     B
0125 C22E01             0041        JP      NZ,TM2
0128 3E07               0042        LD      A,7         ;OUTPUTTING 7 TO
012A D301               0043        OUT     1,A         ;THE CONSOLE WILL
                        0044 ;                          ;RING THE BELL.
012C 067D               0045 INIT:  LD      B,125       ;MULTIPLIER FACTOR.
012E 3E7D               0046 TM2:   LD      A,125       ;COUNT FOR TIMER1
0130 D305               0047        OUT     5,A         ;(125 * 64 USEC = 8 MSEC).
0132 FB                 0048        EI
0133 C9                 0049        RET
                        0050 ;
                        0051 ;
0134                    0052        ORG     200H
0200 2401               0053        DW      TIMER       ;INTERRUPT VECTOR, TIMER1.
```

ANNOTATED SOFTWARE EXAMPLE

TU-ART KIT ASSEMBLY INFORMATION

If you purchased your TU-ART as a kit you will find the assembly to be straightforward. The locations of all the components are clearly marked on the pc board itself. Take care that the parts are positioned and oriented properly before they are soldered in place.

When installing the IC sockets note that no socket should be installed in the position marked "status socket". A socket is only used here if there is a need to change the assignment of status bits in the status word, as described on pages 6 and 7 of this manual.

Also note that three different three-terminal regulators are used in the TU-ART: a 7805, 7812, and 7905. These regulators are not interchangeable. Take caution that each regulator is installed only in the proper position.

It is important that the "+" end of the tantalum capacitors are oriented as marked on the pc board. The cathode (banded) end of the 1N4742 diode (D1) must be oriented to the left. The flat surfaces of transistor Q1 and Q2 should also face the left.

After soldering all parts in place, install the ICs in their sockets. BE VERY CAREFUL THAT EACH PIN OF EVERY IC IS PROPERLY ENGAGED IN ITS SOCKET. After installing the ICs carefully inspect your work.

TU-ART PARTS LIST

Integrated Circuits

IC 1	7442
IC 2	74367
IC 3	74368
IC 4	5501
IC 5	5501
IC 6	74367
IC 7	74368
IC 8	74LS11
IC 9	75189
IC 10	7406
IC 11	75188
IC 12	74LS74
IC 13	74LS08
IC 14	74367
IC 15	74368
IC 16	74367
IC 17	74368
IC 18	74367
IC 19	74367
IC 20	74367
IC 21	74367
IC 22	74LS32
IC 23	74LS08
IC 24	74LS11
IC 25	74LS74
IC 26	7805
IC 27	7812
IC 28	74900
IC 29	74L04
IC 30	74367
IC 31	74367
IC 32	74367
IC 33	74367
IC 34	74LS00
IC 35	74LS157
IC 36	74LS04
IC 37	7905
IC 38	7406
IC 39	74LS04
IC 40	74LS04
IC 41	74LS74
IC 42	74LS00
IC 43	74LS03
IC 44	74373
IC 45	74L04
IC 46	74LS136
IC 47	74LS136
IC 48	74LS74

Capacitors

C1	0.1 uF
C2	.05 uF
C3	0.1 uF
C4	0.1 uF
C5	.05 uF
C6	10 uF
C7	0.1 uF
C8	0.1 uF
C9	10 uF
C10	0.1 uF
C11	0.1 uF
C12	10 uF
C13	0.1 uF
C14	0.1 uF
C15	0.1 uF
C16	0.1 uF
C17	0.1 uF
C18	75 pF
C19	75 pF
C20	10 uF
C21	.05 uF
C22	10 uF
C23	30 pF
C24	0.1 uF
C25	0.1 uF
C26	0.1 uF
C27	0.1 uF
C28	10 uF
C29	10 uF
C30	0.1 uF
C31	0.1 uF
C32	300 pF

Diodes/Transistors

D1	1N4742 Zener
Q1	2N3906
Q2	2N3906

Resistors

R1 1K
R2 390
R3 470
R4 1.5K
R5 1.5K
R6 680
R7 18K
R8 18K
R9 470
R10 1.5K
R11 1.5K
R12 680
R13 390
R14 1K
R15 1K
R16 330
R17 330
R18 47
R19 47
R20 220
R21 1K
R22 1K
R23 1K
R24 1K

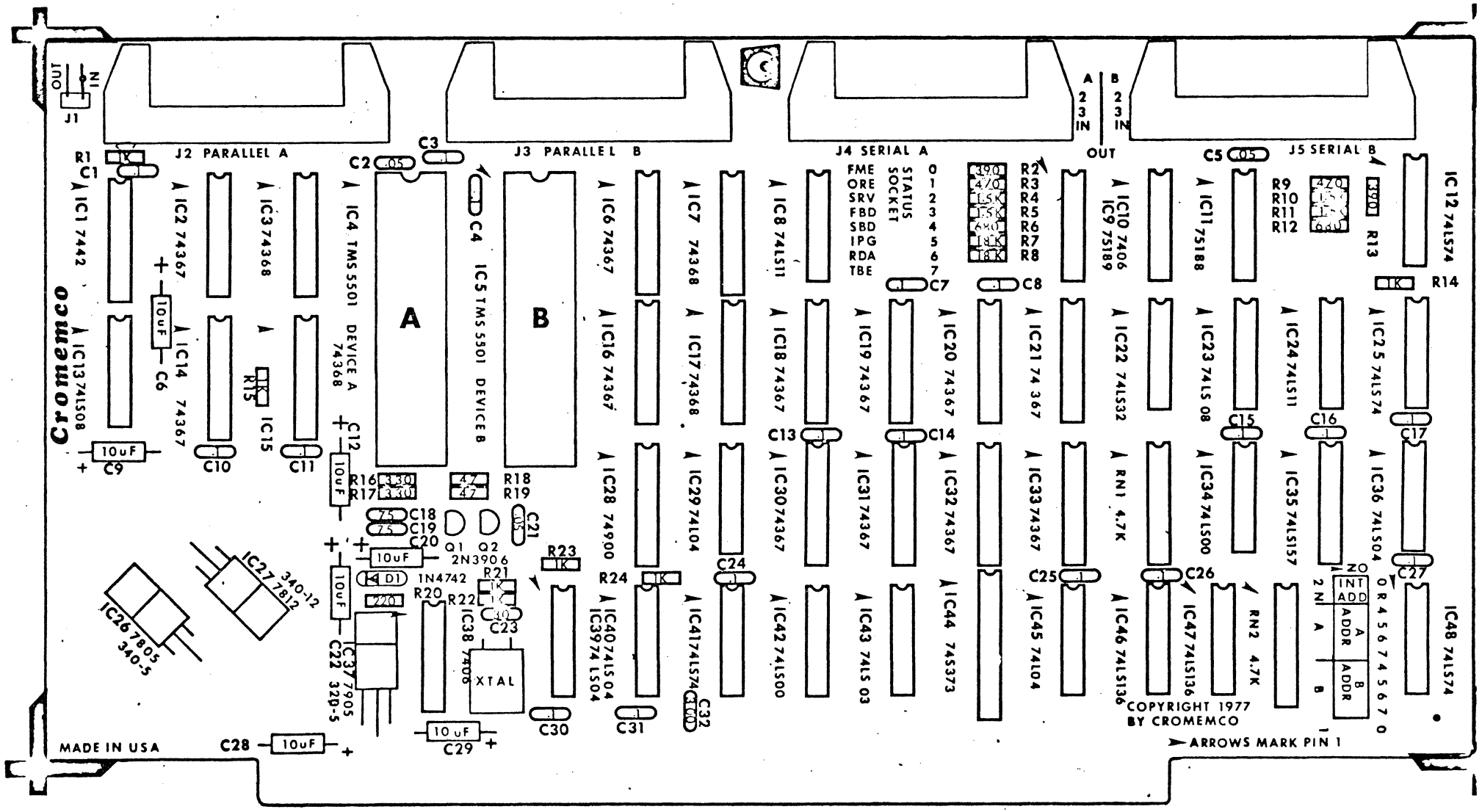
RN1 4.7K DIP (15 resistors)
RN2 4.7K DIP (15 resistors)

IC Sockets

2 40 pin sockets
1 20 pin socket
23 14 pin sockets
21 16 pin sockets

Miscellaneous

Printed circuit board
10 pole DIP switch
4 26-pin cable sockets
1 Heatsink
5 6-32 screws
5 6-32 nuts
8 2-56 screws
8 2-56 nuts
Manual and Schematic Diagram



TU-ART PARTS PLACEMENT DIAGRAM

TU-ART LEGEND REV C

TU-ART THEORY OF OPERATION

I. INTRODUCTION

The TU-ART has ten functional blocks supporting the TMS 5501s:

A. Power Supply Three IC regulators and a zener diode are used to generate ±5 and ±12 volts.

B. Crystal Controlled Clock An 8 MHz crystal oscillator is used as an on-board reference to control the internal state machine and to drive the Ø1 and Ø2 clocks of the TMS 5501s.

C. Address Select Two four-bit address comparators generate base address select signals when the four most significant device address bits of an input or output instruction agree with one of the two base address switch settings on the TU-ART. The base address select signals enable the appropriate TMS 5501 (depending on the current state of the Address Reverse multiplexer).

D. Function Decode The four function address pins on the TMS 5501s are driven by a read only memory addressed by the lower four bits of the S-100 address bus and status signal $\overline{WO}$. The ROM also generates signals for internal bus control.

E. State Sequencer The internal state sequencer starts up whenever the TU-ART is addressed and cycles the internal bus through an 8080 M3-like sequence. The sequence starts with a SYNC pulse to the 5501s while the internal data bus is strobed with status information appropriate to the type of cycle requested by the processor (IO read, IO write, or Interrupt Acknowledge); continues while data is written or read; and terminates after signalling READY to the processor.

F. Status Strobe Data bus pins DØ and D1 are controlled by the status strobe circuit during internal SYNC time to select the proper TMS 5501 operation.

G. Bus Multiplexers The internal data bus is time multiplexed (for status information), direction multiplexed (depending on the type of cycle: read or write), and path multiplexed (depending on the particular read-type function being performed) under control of the state generator and three-state bus drivers.

H. Serial Interface The TTL level serial output signal from the TMS 5501s is converted to EIA RS/232 levels and to a teletype compatible current switch. Serial input may be from either EIA or teletype.

I. Parallel Interface TTL Bus buffers drive the parallel ports. Handshaking signals are controlled by the function decoder ROM.

J. Priority Chain A ripple priority resolver controls Data bit DØ (INTA) on each TMS 5501 during SYNC time. This prevents both devices from responding to an Interrupt Acknowledge cycle from the processor when both devices have active interrupt requests. The priority chain is expandable to multiple boards.

These ten blocks, which are listed in the approximate order of attack for troubleshooting, will be discussed in detail below.

II. Power Supply

The TMS 5501s require three power supplies: V_{CC} = +5, V_{DD} = +12, and V_{BB} = -5. A -12V source is created by zener diode D1 for the EIA line driver and receiver IC's. The +12 supply is used by the EIA line drivers, the TTY interface, and the Ø1, Ø2 clock drivers. The -5 supply is used by the TTY interface.

III. Crystal Controlled Clock

An 8.000 MHz crystal oscillator generates the TU-ART's timebase. A two-phase, 2MHz clock is derived from IC41P8 ($\overline{\text{Ø2TTL}}$) and IC42P6 ($\overline{\text{Ø1TTL}}$). These signals are followed by high voltage inverters to generate the 12 volt clocks for the TMS 5501s. Transistors Q1 and Q2 form edge-active pullups for the inverters. A 75 pf - 330 ohm differentiator network on the base of each transistor couples a spike from the falling edge of the TTL input into the base. This switches the transistor on briefly and pulls the collector to +12 volts. A 47 ohm series resistor in the clock lead reduces ringing and overshoot. The rising edge of the TTL input turns on the 7406 inverter which pulls the collector of the transistor (now off) back to ground.

The state generator is clocked by Ø2TTL and $\overline{\text{Ø2TTL}}$ outputs from IC41P9 and IC41P8.

Clock waveforms are summarized in Figure I.

IV. Address Select

Four-bit address comparison is performed by open collector exclusive or gates IC46 and IC47. Incoming address lines are deglitched and inverted by 74L04 inverters, then ex-ored with 4 bits from the DIP switch base address select positions. A closed switch matches a "1" on the address bus; an open switch matches a "0" on the Address bus; when all four bits match and SOUT or SINP is active then the open collector wired - and node will go high. If the node at RN2P7 is high Base Address B is being selected. If RN2P5 is high Base Address A is being selected. When Device A is addressed IC43P6 pulls down the Device B select node to prevent bus conflict if both base addresses accidentally have been set equal. When either Device select is active

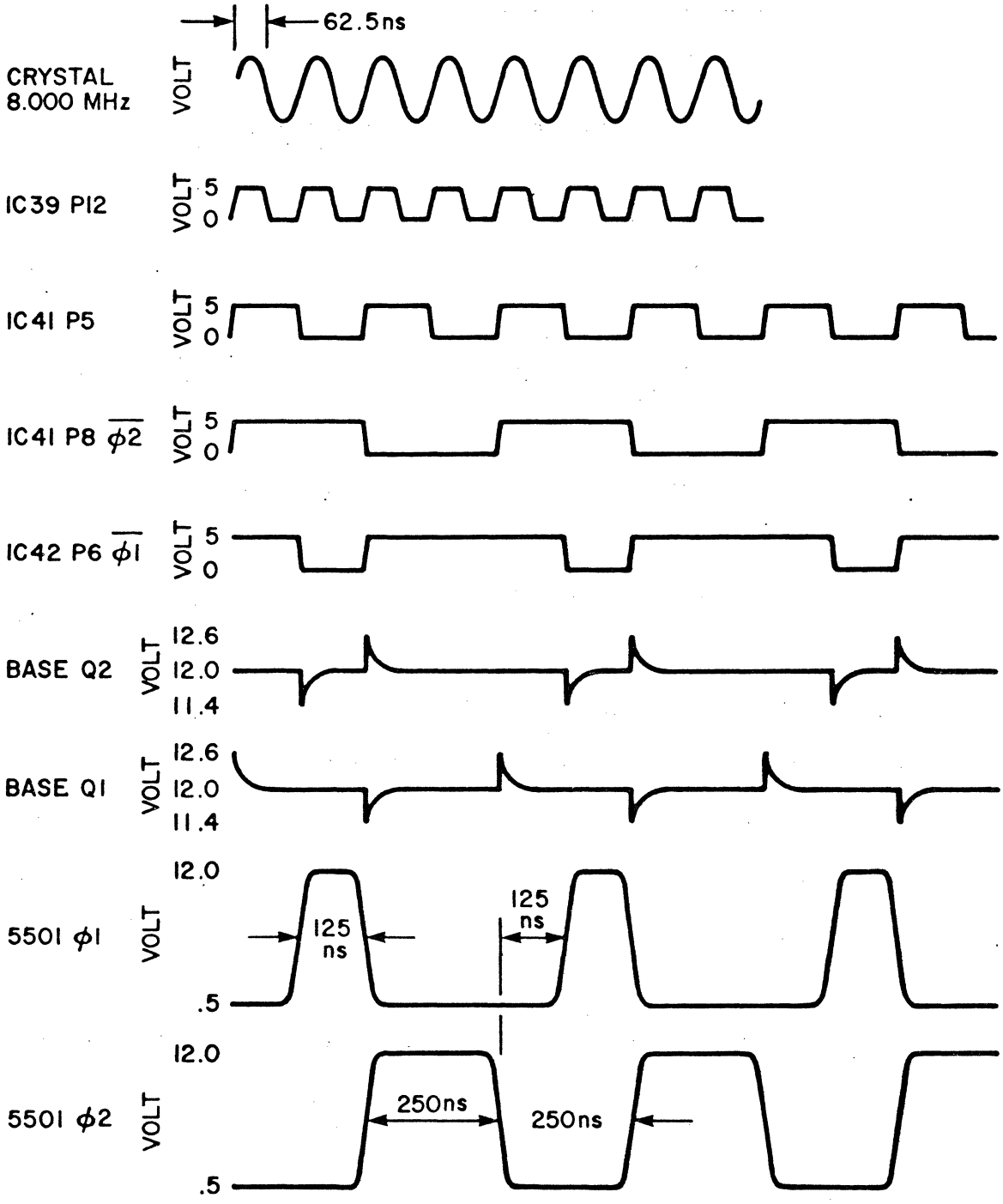


Figure I - TU-ART CLOCK WAVEFORMS

IC40P10 goes low, enabling the Function Decoder ROM. Multiplexer IC35 performs Base Address reversing when its select pin goes low. In the normal case Device A select enables the CE driver of IC4, while Device B select enables the CE driver of IC5. Base address reversing enables IC5 in IC4's place and vice versa. The select pin of the MUX, IC35P1 is controlled by the signal applied to J2P1 or J3P1; or, if DIP Switch 2 is closed, by IC4P31 (the MSB of Device A's output parallel port).

V. Function Decode

TTL PROM IC28 is enabled when IC28P15 goes low (which occurs at the beginning of Input and Output cycles). IC28 is not enabled during interrupt acknowledge. When IC28 is enabled, it supplies function address signals to the 4 address pins of the 5501s. IC28P5 goes low during I/O operations involving the parallel ports and drives IC1, a decoder chip which generates Input and Output strobe signals. IC28P6 goes low during Output cycles. This signal controls the incoming bus buffers, generates a state-cycle request by pulling down IC24P10, and is strobed on the internal data bus bit D1 at SYNC time by IC43P3. IC28P7 goes low during INPUT cycles. This signal controls the outgoing bus drivers and generates a state-cycle request by pulling down IC24P9. This signal is not active (floats) during INTA cycles. I28P9 goes low when the status port of the TMS 5501s is read. This signal controls an internal data path from the TMS 5501s to the output data latch, IC44.

VI. State Sequencer

The heart of the TU-ART is the state sequencer, a four-stage shift register which times the status drivers and data in/out circuits to form an 8080-like internal bus. The input to the state sequencer, IC25P2, is the signal from IC36P6 (I O READ + IOWRITE + INTERRUPT ACKNOWLEDGE). While this signal is low, the state sequencer is held

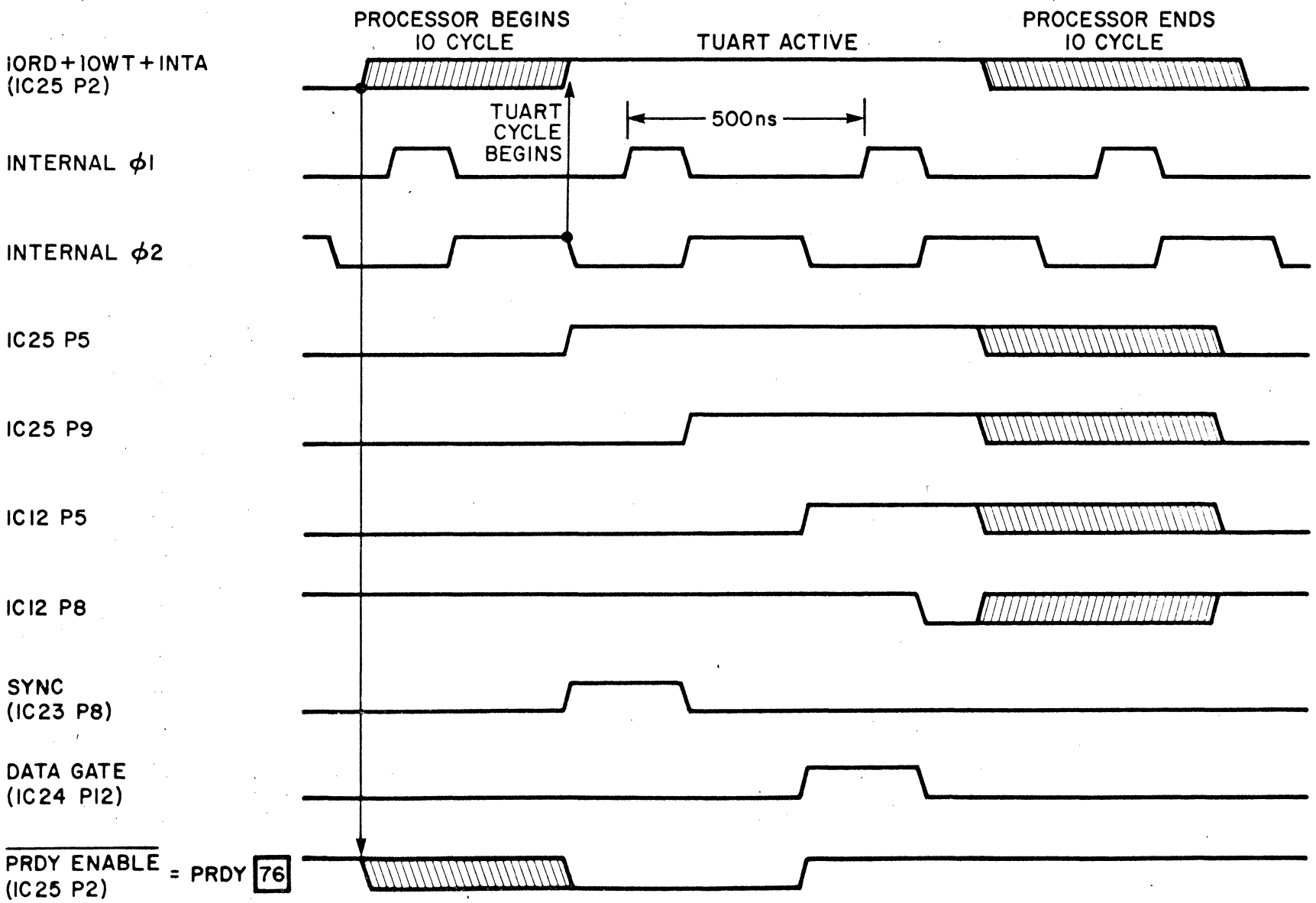


Figure II - TU-ART STATE SEQUENCER TIMING

in a reset state by direct clear pins 1 and 13 of ICs 25 and 12. When the input goes high a high level will be shifted to IC25P5 at the first falling edge of Ø2. IC23P8 then goes high, generating a SYNC signal at Pin 19 of both TMS 5501s and turning on status strobe driver IC18 through IC40P6 and IC43P1.

The state sequencer is now clocked by the rising edge of Ø2, shifting a high level to IC25P9. IC23P10 goes low and remains low until the state sequencer is reset at the end of the I/O cycle. The status strobe drivers are shut off. The TMS 5501 now arranges internal data paths according to the address and status information it received during SYNC time. If the TU-ART is in an IOWRITE cycle the S-100 DO bus receivers IC18 and IC30 are enabled.

The state sequencer is clocked for a third time by Ø2 falling edge, propagating the high level at IC25P9 to IC12P5. The Gate input of the DI bus latch is raised (IC44P11). The PRDY driver IC16 is disabled, signalling "READY" to the CPU, and releasing the bus from its WAIT condition.

The final change in state occurs on the rising edge of Ø2 when IC12P8 goes low. This shuts off the DI latch gate. The state sequencer has completed its cycle and remains in this state until the processor terminates the I/O cycle.

VII. Status strobe

The TMS 5501s have no control pins for DBIN or $\overline{WR}$; instead the ICs monitor bits DØ and DI of the data bus during SYNC for status information. If DØ is high during SYNC, an Interrupt Acknowledge cycle is beginning, and the 5501 will send data to the bus during "T3" of the

cycle. If D1 is high an IOREAD operation is beginning and the 5501 whose CE pin was high during SYNC will access the internal register addressed by A3-AØ and present data to the bus at "T3" of the cycle. If D1 is low during SYNC, an IOWRITE operation is beginning and the 5501 whose CE pin was high during SYNC will latch data from the bus during "T3" of the cycle.

Bit D1 is controlled by an open collector nand, IC 43, which is strobed by SYNC. Bit DØ is split into DØA and DØB so that INTA can be sent to the TMS 5501s individually. This is necessary because CE no longer selects the chip during interrupt acknowledge. Three-state driver IC18 controls DØA and DØB during SYNC.

VIII. Bus Multiplexers

The internal data bus which connects the two TMS 5501s will float while idle. At the beginning of a cycle it is strobed by the status drivers as described in section VII. Following status the bus assumes one of five configurations:

A. IOWRITE cycle: The S-100 DO bus receivers drive the internal data bus during WR • (T $\geq$ T2).

B. IOREAD (EXCEPT READ STATUS PORT): The internal data bus is buffered by a set of permanently-enabled 74367 sections, then passed through another set of 74367s, enabled by the assertion of READ and $\overline{\text{STATUS}}$. These 74367s drive the output latch IC44 which latches during T3 of the internal cycle. IC44 has three state output drivers built in which drive the S-100 DI bus during DBIN • IOACTIVITY.

C. IOREAD STATUS: The buffered internal data bus passes through the status bit select pocket where bits from the 5501 may be arranged

arbitrarily in order to control flag bit assignments. The "scrambled" bits are then passed through 74367s which have been enabled by $\overline{\text{STATUS}}$ going low. The output latch operates as before.

D. INTA Mode 2 (Z-80): During a mode 2 INTA the buffered internal data bus bibs D3-D5 plus INTA B plus A7 A6 and A5 from Base address A form inputs to a set of 74367s which drive the output latch.

E. INTA MODE Ø (8080): During MODE Ø INTA the buffered internal data bus bits D3-D5 are routed through 74367s straight to the output latch. The remaining bits are passively pulled high.

IX. Serial Interface

Transmit output from the TMS 5501 is inverted to RS232 levels by IC11 (1488). Output is also provided from a 7406 high voltage inverter for grounding a 20 mA current source or for TTL level output. The RS232 output idles at -12v, the 7406 output idles at ground (conducting).

Receiver input is taken from an RS 232 line receiver, IC9 (1489). IC9 converts RS232 levels to TTL. When a TTY keyboard is used, it switches the bias voltage on IC9 from +12 to -5 which causes TTL level switching at the output.

The output of the 1489 idles at +5 volts.

X. Parallel Interface

Parallel inputs to the TMS 5501 are TTL buffered by 74367s. Parallel outputs are inverted and buffered by 74368s to keep positive logic. The 74368s may be three stated by grounding $\overline{\text{DISABLE}}$. Strobe signals are decoded by IC1.

XI. Priority Chain

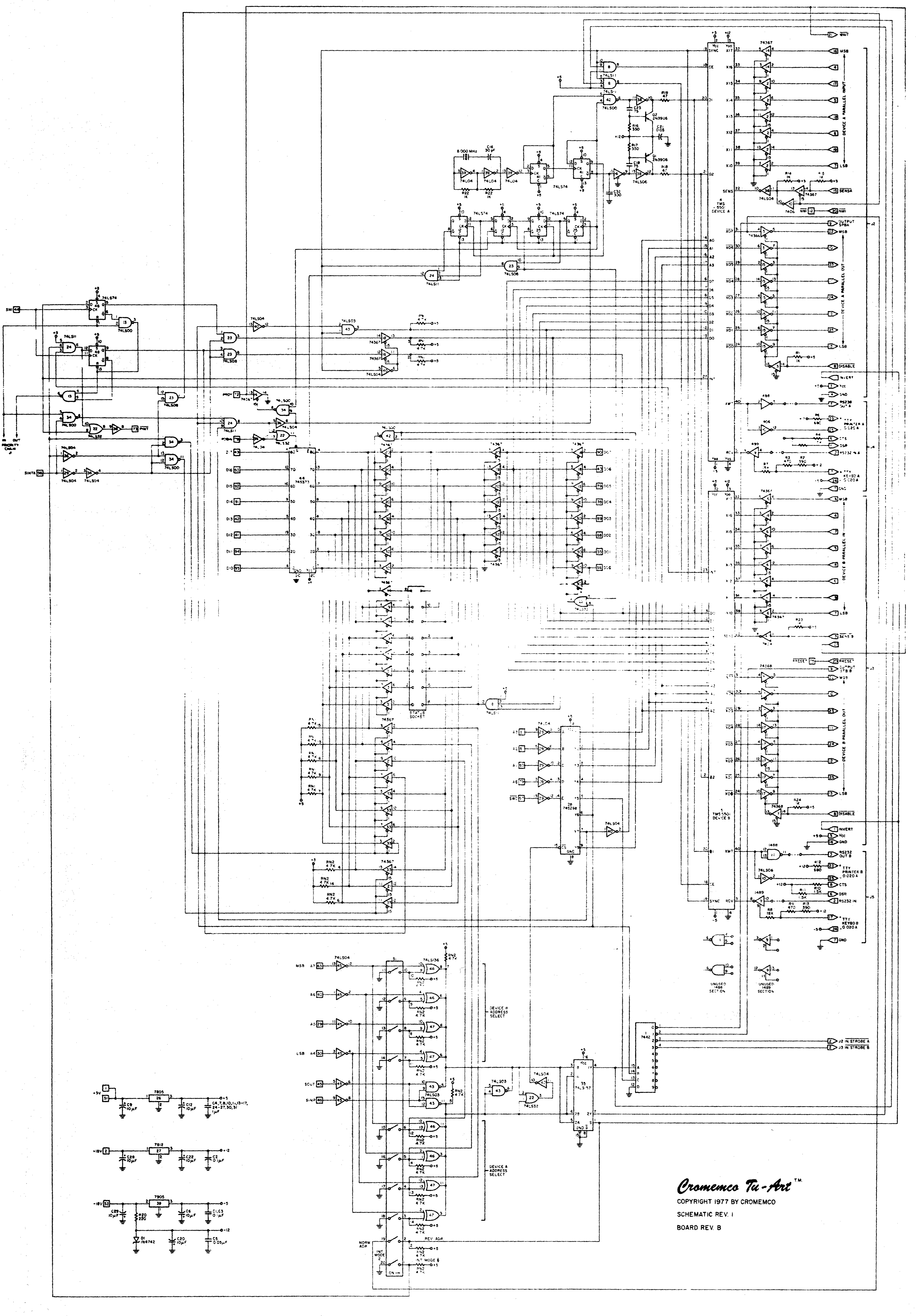
The TU-ART will respond to an Interrupt Acknowledge cycle from the processor when three conditions are satisfied: 1) The processor has raised SINTA, the Interrupt Acknowledge status signal 2) One of the TMS 5501s is requesting interrupt (high level on IC4P23 or IC5P23) and 3) No other device higher up the priority chain is requesting an interrupt. The priority chain input at J1 is used to clear IC48, the INTA enable flip flop. Suppose IC4 (Device A) requested an interrupt at the same time as IC5 (Device B). If $\overline{\text{Priority IN}}$ was being held low by a higher priority TU-ART, both sections of IC48 would remain cleared, disabling IC23P5 and IC23P6 from generating SINTA status bits. When $\overline{\text{Priority IN}}$ is allowed to float to +5, the next M1 occurrence will clock the two sections of IC48 (M1 may be the start of an INTA cycle, though it doesn't have to be). Both IC48P5 and IC48P9 go high momentarily because both DEVICE A and Device B have interrupts pending. However IC48P6 ripples through IC13P3 to force IC48P9 low in exactly the same manner as $\overline{\text{PRIORITY IN}}$ from J1. Thus only DEVICE A actually receives the INTA status bit and no bus conflict is allowed.

WARRANTY

Your factory-built TU-ART is warranted against defects in materials and workmanship for a period of 90 days from the day of delivery. We will repair or replace products that prove to be defective during the warranty period provided that they are returned to Cromemco. No other warranty is expressed or implied. We are not liable for consequential damages.

Should your factory-built TU-ART fail after the warranty period it will be repaired, provided that it is returned to Cromemco, for a fixed service fee. We reserve the right to refuse to repair any product that in our opinion has been subject to abnormal electrical or mechanical abuse. The service fee is currently $35 and is subject to change.

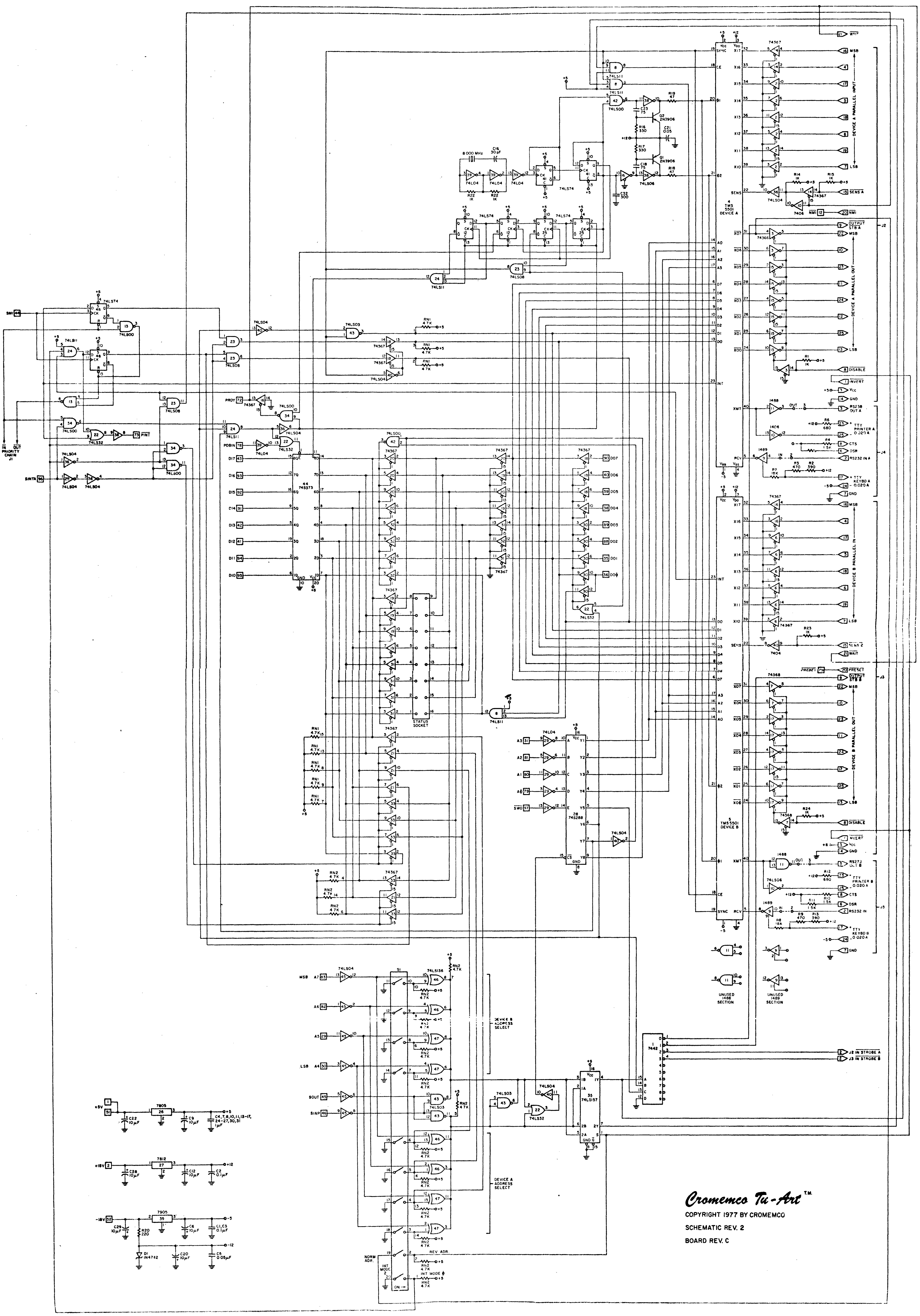
Your assembled TU-ART kit will be repaired, provided that it is returned to Cromemco, for a fixed service fee. We reserve the right to refuse to repair any kit that in our opinion has not been assembled in a workmanlike manner or has been subject to abnormal electrical or mechanical abuse. Payment of the service fee must accompany the returned merchandise. The service fee is currently $35 and is subject to change.



Cromemco Tu-Art™

SCHEMATIC REV. 1

BOARD REV. B


Cromemco Tu-Art T.M.
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SCHEMATIC REV. 2
BOARD REV. C
DEVICE A PARALLEL INPUT
DEVICE A PARALLEL OUT
DEVICE B PARALLEL IN
DEVICE B PARALLEL OUT
TMS 5501 DEVICE A
TMS 5501 DEVICE B
STATUS SOCKET
DEVICE B ADDRESS SELECT
DEVICE A ADDRESS SELECT
UNUSED 1488 SECTION
UNUSED 1489 SECTION
J2 IN STROBE A
J3 IN STROBE B
IN OUT PRIORITY CHAIN J1